

3U cPCI to PMC Active 64 Bit Carrier

Product Description:

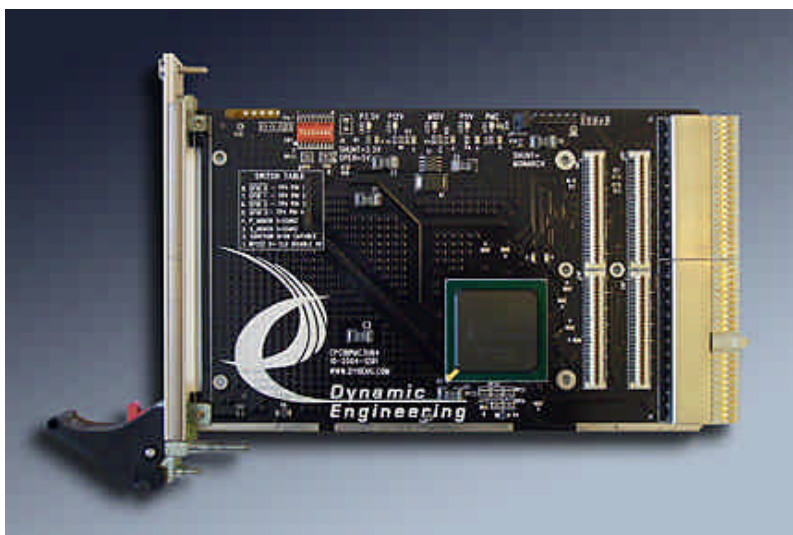
The cPCIBPMC (cPCI to PMC) adapter / carrier converter card provides the ability to install a PMC card into a standard cPCI slot. The cPCIBPMC has a PMC card slot mounted to a universal 3U 4HP cPCI card. The cPCIBPMC is a 0 - 70C board design based on the 21154 bridge. It is suitable for 32/64 with 33/ 66 MHz bus operation. The 3U card is wired for 64 bit PCI operation with pull-ups on the control lines to allow use in a 32 bit system. The PMC bezel connector is mounted through the cPCI mounting bracket.

The PCI bus is interconnected to the PMC via 64 bit 66 MHz capable layout. The supplied dip-switch is used to control the bridge configuration. The user can select the clock rate, [33/66] on both buses and has access to the GPIO bits. PME and the Interrupt request lines are routed from the PMC to the cPCI connector.

The PCI VIO is interconnected to the primary side of the bridge. The secondary side of the bridge has programmable VIO allowing 5V PMCs to be used in 3V systems and vice-versa. The voltage select pins are not installed on the cPCIBPMC. The bridge will automatically adapt to the PCI bus reference voltage. Many PMCs are "universal" and can work with 3.3 or 5V cPCI backplanes. The secondary side has a shunt for the user to select 5V or 3V operation.

The cPCIBPMC follows the PMC specs for maximum power consumption and heat dissipation (7.5 watts). The power is routed from the cPCI to PMC connectors with mini-planes each of which is rated for more than the maximum PMC draw. 3.3, 5, VIO, +12, -12

cPCI J2 has two definitions - in a 64 bit PCI implementation J2 has the upper A/D and control signals and in a 32 bit PCI implementation J2 has the rear panel IO. The cPCIBPMC3U64 has the upper part of the PCI bus connected to J2. In addition the commonly used Ethernet and I2C pins from the Jn4 and Jn1 are connected to unused pins on J2 to allow rear panel IO for those signals. Please refer to the manual for the signal definitions.



Top view of cPCIBPMC3U64-IO carrier

Ordering

PCI_cPCIBPMC3U64

3U cPCI to PMC Carrier, active 64Bit, with front I/O

PCI PMC Carrier Specifications

Key Features

- Size - 3U 4HP cPCI
- PMC compatible slot - 1 PMC Slot provided.
- Clocks - cPCI bus can operate at 66 or 33 MHz. The PMC must be 66 MHz capable for 66 MHz operation to work properly. User switch to allow or disable 66 MHz. operation
- Access Width - Standard cPCI byte lanes supported for byte, word and long access dependent on installed PMC. 64 or 32 bit operation supported.
- Software Interface - PMC register definitions as defined by installed hardware. No software set-up required by cPCIBPMC.
- Interrupts - INTA, B, C, D routed to cPCI connector from PMC.
- Signal Conditioning - Secondary side PCI signals are routed and terminated IAW the PCI specification
- Power - +5, +3.3, +12, -12V, VIO supplied to PMC.
- Typ. PMC power - 7.5 W
- Max. PMC power - 25 W
- Max. Carrier power - 2.2W
- VIO - Bridge primary PCI IO Voltage is set by the PCI backplane. Secondary side VIO is programmable by the user.
- Thermal - The cPCIBPMC is a low power design with minimal heat dissipation for optimal PMC performance.
- IO Interface - Front Bezel IO supported at cPCI bracket. Partial Jn4 "user IO" supported [Ethernet and I2C] with interconnection to J2.
- LEDs - +3V, +5V, +12V, -12V and Busmode 1.
- JTAG - JTAG header connected to PMC supplied. JTAG pin definitions are in the silkscreen.